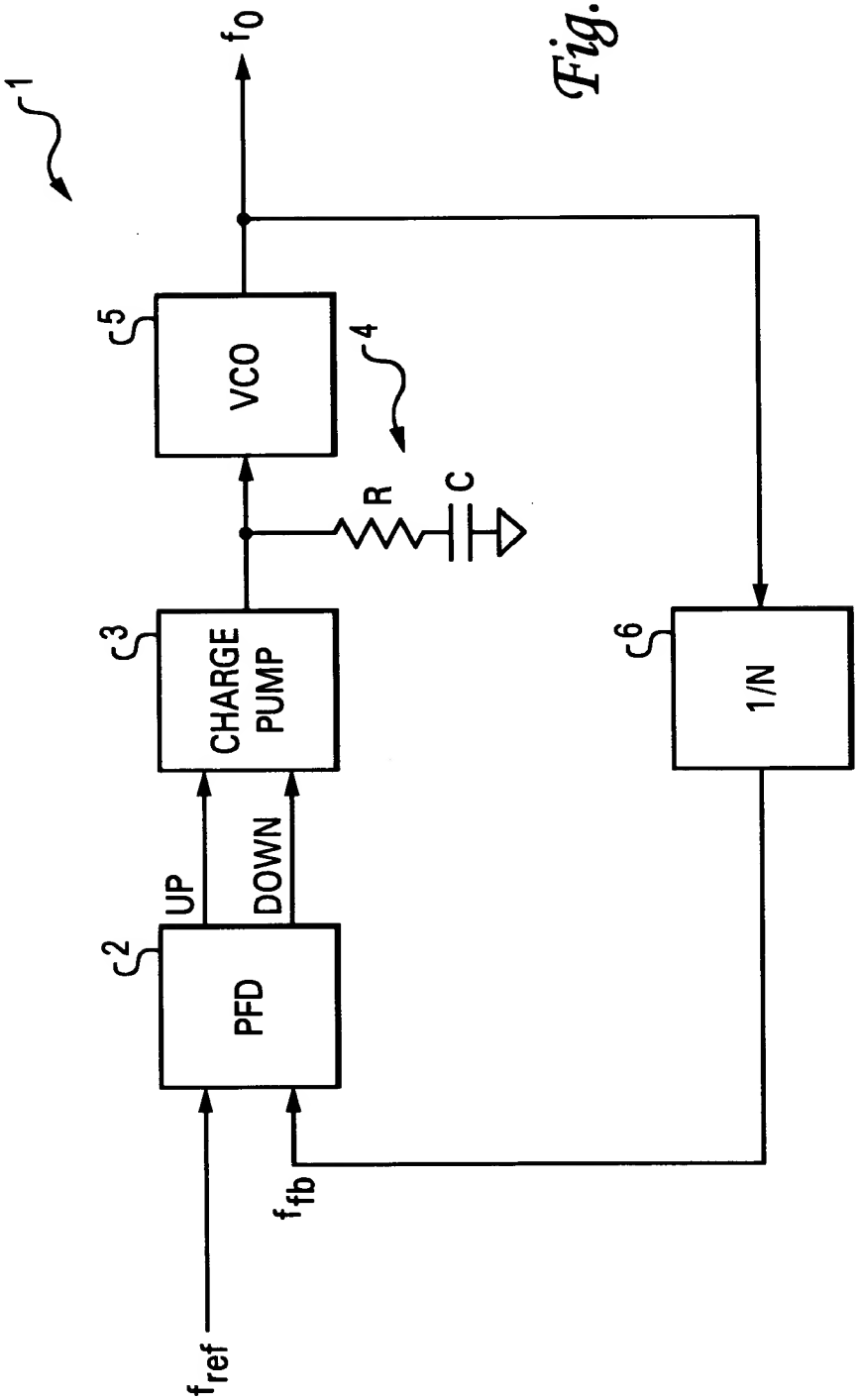

Fig. 1 Prior Art

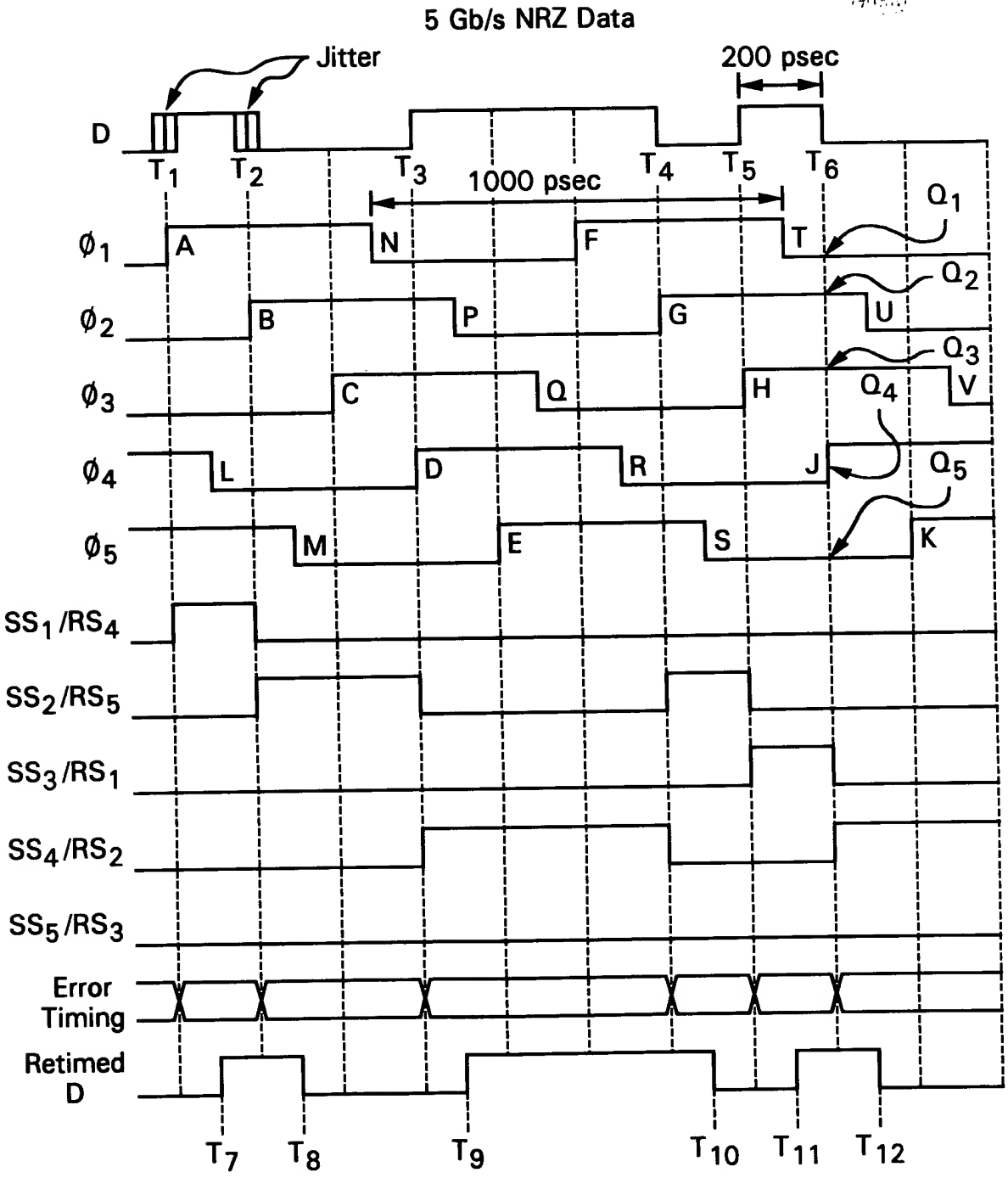
5 Gb/s NRZ Data
Jitter
200 psec
D
T1
T2
T3
1000 psec
T4
T5
T6
Q1
Q2
Q3
Q4
Q5
ϕ1
ϕ2
ϕ3
ϕ4
ϕ5
A
N
F
T
B
P
G
U
C
Q
H
V
L
D
R
J
M
E
S
K
SS1/RS4
SS2/RS5
SS3/RS1
SS4/RS2
SS5/RS3
Error Timing
Retimed D
T7
T8
T9
T10
T11
T12

Fig. 2

Q_1	Q_2	Q_3	Q_4	Q_5	SynchState	RetimeState
X	0	0	1	1	1	4
1	X	0	0	1	2	5
1	1	X	0	0	3	1
0	1	1	X	0	4	2
0	0	1	1	X	5	3

Fig. 3

SynchState	Q_1	Q_2	Q_3	Q_4	Q_5	Clock Late Wrt Data
1	0	0	0	1	1	1
1	1	0	0	1	1	0
2	1	0	0	0	1	1
2	1	1	0	0	1	0
3	1	1	0	0	0	1
3	1	1	1	0	0	0
4	0	1	1	0	0	1
4	0	1	1	1	0	0
5	0	0	1	1	0	1
5	0	0	1	1	1	0

Fig. 4

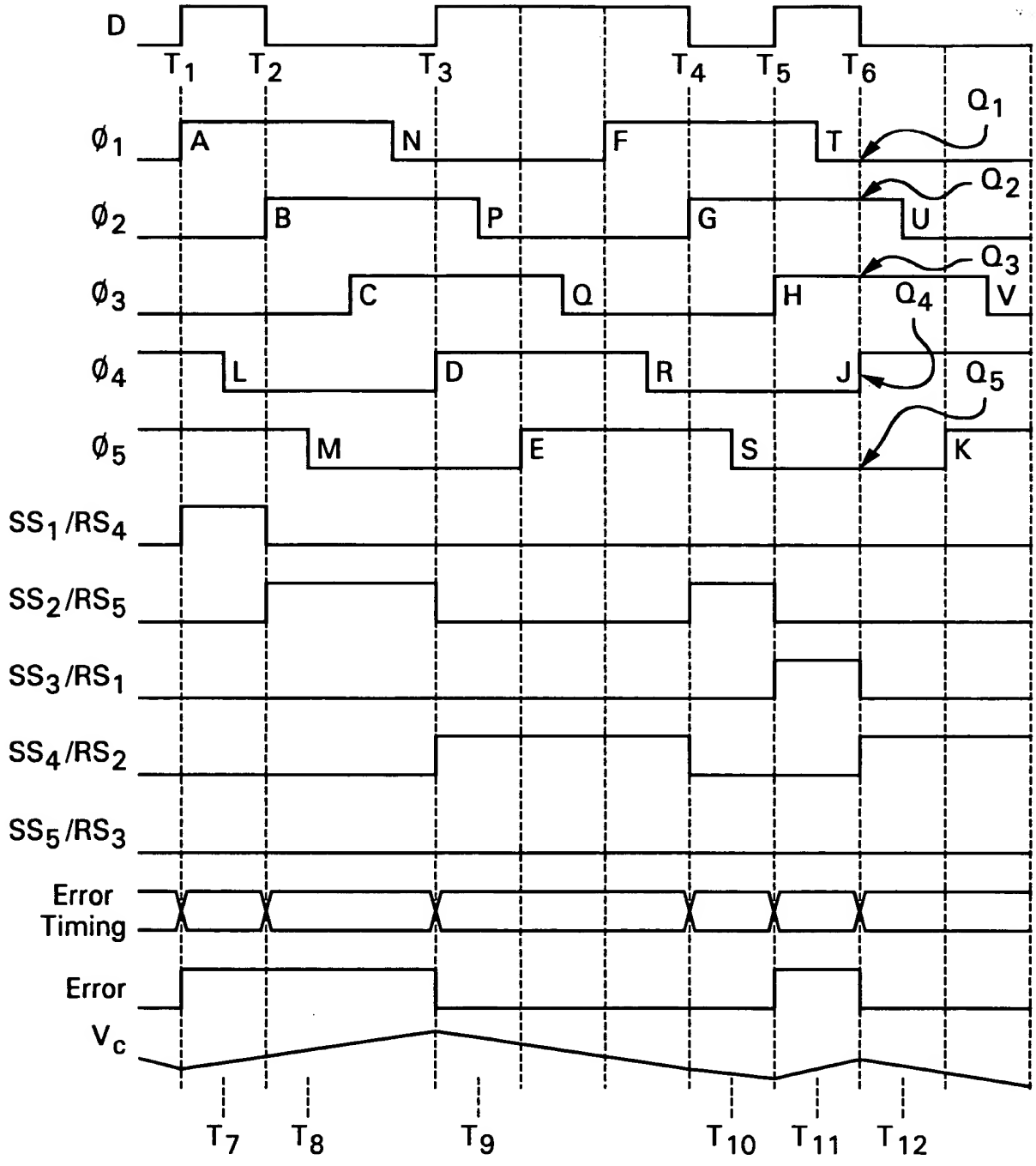
D
T1
T2
T3
T4
T5
T6
Ø1
A
N
F
T
Q1
Ø2
B
P
G
U
Q2
Ø3
C
Q
H
V
Q3
Q4
Ø4
L
D
R
J
Q5
Ø5
M
E
S
K
SS1/RS4
SS2/RS5
SS3/RS1
SS4/RS2
SS5/RS3
Error Timing
Error
Vc
T7
T8
T9
T10
T11
T12

Fig. 5

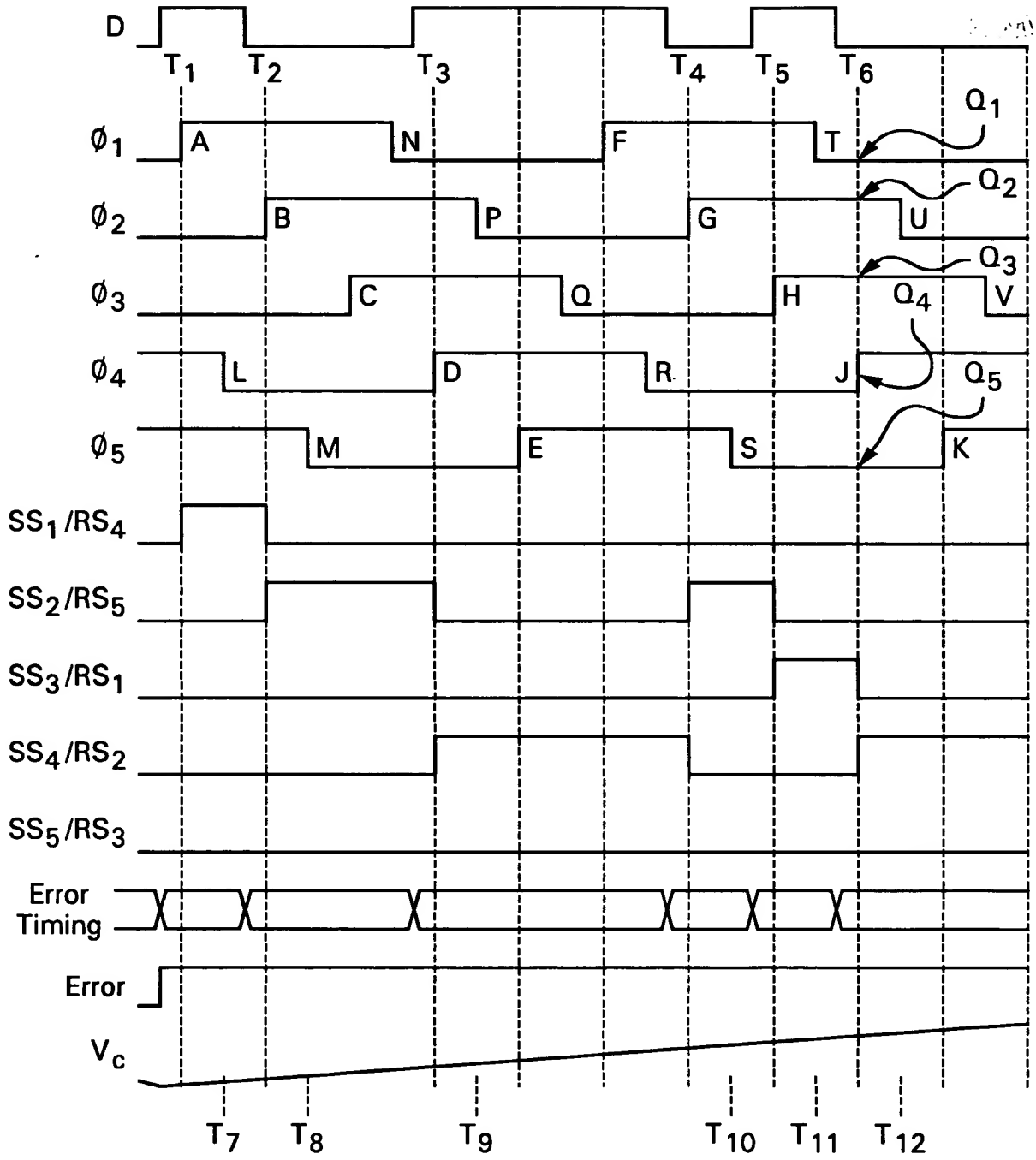
D
T1
T2
T3
T4
T5
T6
Ø1
A
N
F
T
Q1
Ø2
B
P
G
U
Q2
Ø3
C
Q
H
Q4
V
Q3
Ø4
L
D
R
J
Q5
Ø5
M
E
S
K
SS1/RS4
SS2/RS5
SS3/RS1
SS4/RS2
SS5/RS3
Error Timing
Error
Vc
T7
T8
T9
T10
T11
T12

Fig. 6

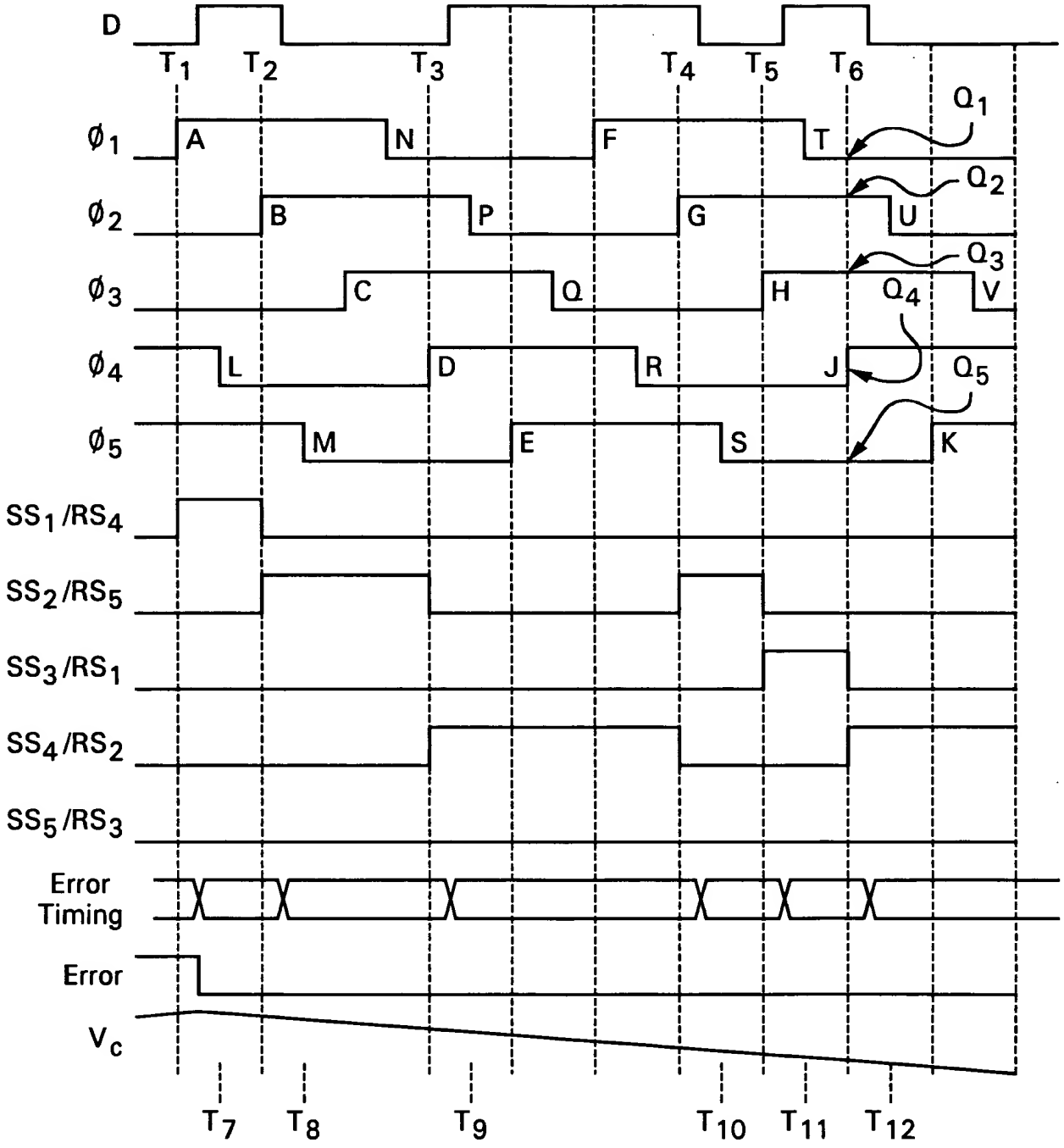
D
T1
T2
T3
T4
T5
T6
Q1
Q2
Q3
Q4
Q5
ϕ1
A
N
F
T
ϕ2
B
P
G
U
ϕ3
C
Q
H
V
ϕ4
L
D
R
J
ϕ5
M
E
S
K
SS1/RS4
SS2/RS5
SS3/RS1
SS4/RS2
SS5/RS3
Error Timing
Error
Vc
T7
T8
T9
T10
T11
T12

Fig. 7

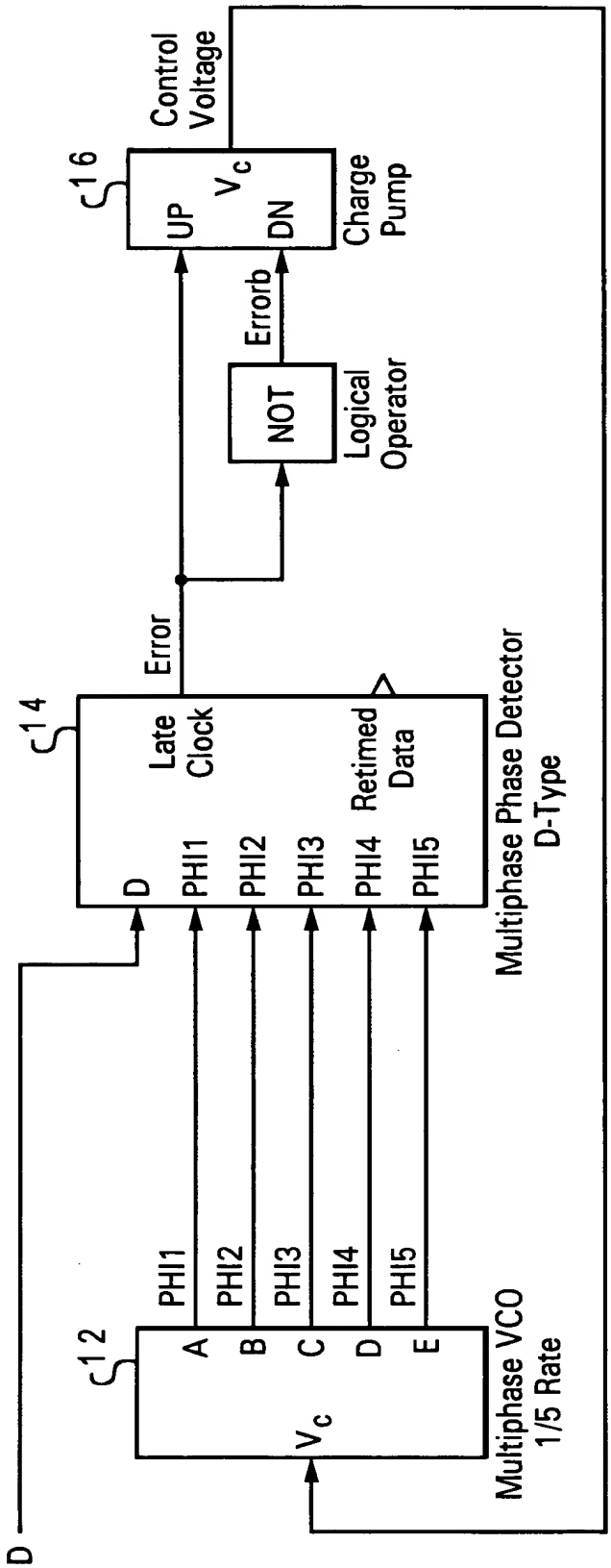
10
12
Multiphase VCO
1/5 Rate
V_c
A
B
C
D
E
PHI1
PHI2
PHI3
PHI4
PHI5
D
14
Multiphase Phase Detector
D-Type
D
PHI1
PHI2
PHI3
PHI4
PHI5
Late
Clock
Retimed
Data
Error
16
Charge
Pump
UP
DN
V_c
Control
Voltage
Logical
Operator
NOT
Errorb

Fig. 8

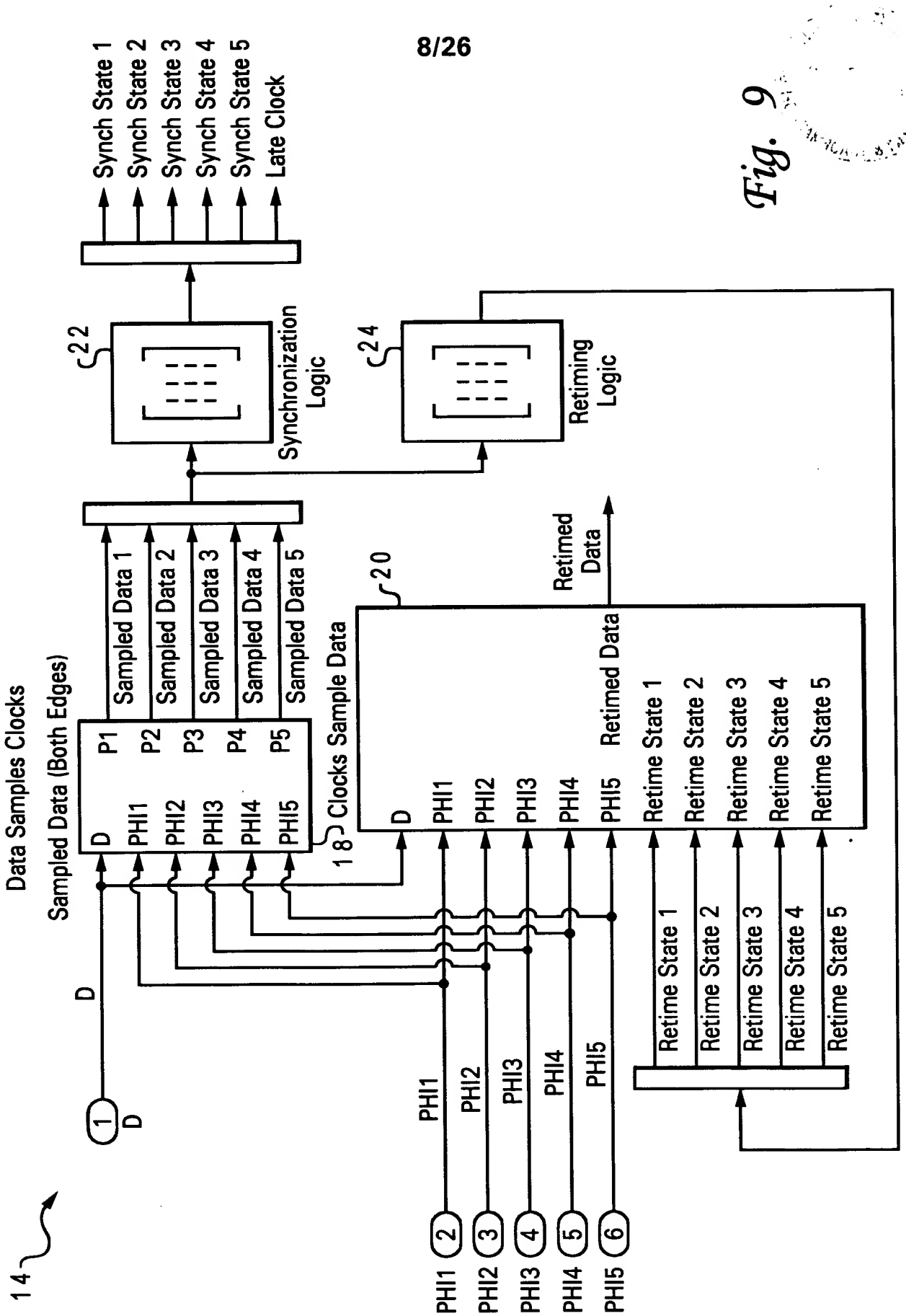
14
Data Samples Clocks
Sampled Data (Both Edges)
D
PHI1
PHI2
PHI3
PHI4
PHI5
P1
P2
P3
P4
P5
Sampled Data 1
Sampled Data 2
Sampled Data 3
Sampled Data 4
Sampled Data 5
18
Clocks Sample Data
20
Retimed Data
Retime State 1
Retime State 2
Retime State 3
Retime State 4
Retime State 5
22
Synchronization Logic
24
Retiming Logic
Synch State 1
Synch State 2
Synch State 3
Synch State 4
Synch State 5
Late Clock
1
2
3
4
5
6

Fig. 9

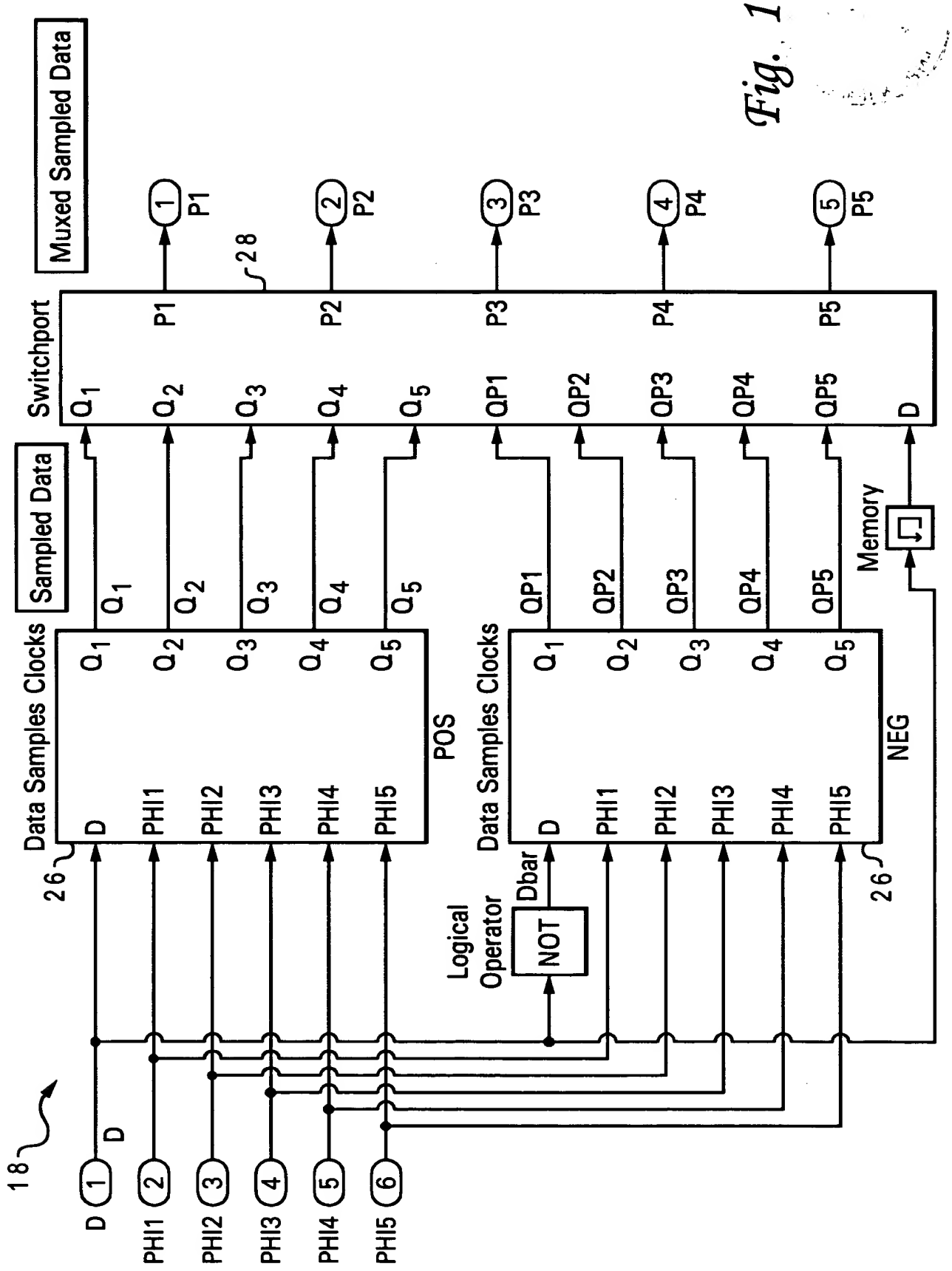
Muxed Sampled Data
Switchport
Sampled Data
Data Samples Clocks
POS
NEG
Logical Operator
NOT
Dbar
Memory
D
PHI1
PHI2
PHI3
PHI4
PHI5
P1
P2
P3
P4
P5
Q1
Q2
Q3
Q4
Q5
QP1
QP2
QP3
QP4
QP5
18
26
28

Fig. 10

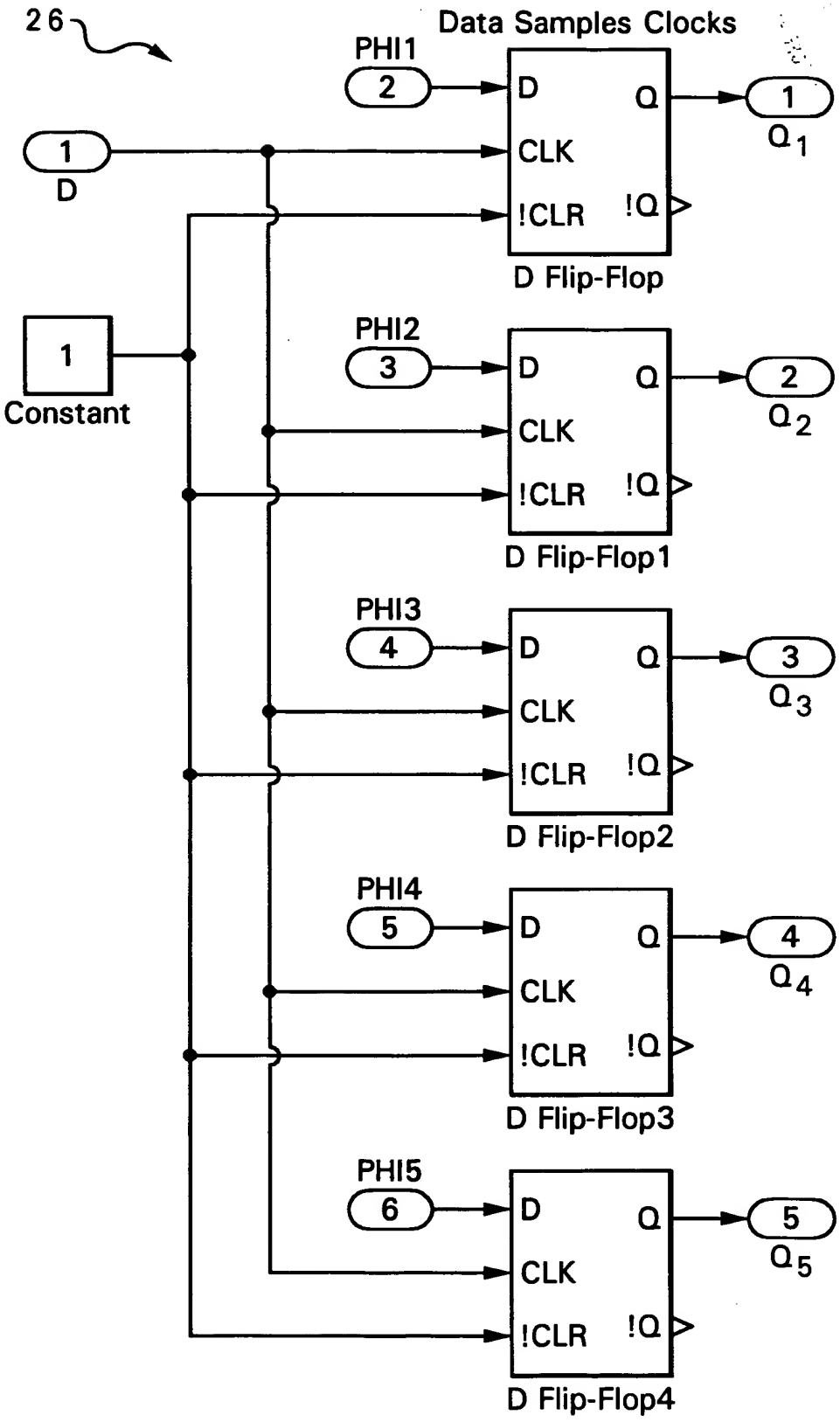
26
Data Samples Clocks
PHI1
2
D
Q
1
Q1
1
D
CLK
!CLR
!Q
D Flip-Flop
PHI2
3
D
Q
2
Q2
1
Constant
CLK
!CLR
!Q
D Flip-Flop1
PHI3
4
D
Q
3
Q3
CLK
!CLR
!Q
D Flip-Flop2
PHI4
5
D
Q
4
Q4
CLK
!CLR
!Q
D Flip-Flop3
PHI5
6
D
Q
5
Q5
CLK
!CLR
!Q
D Flip-Flop4

Fig. 11

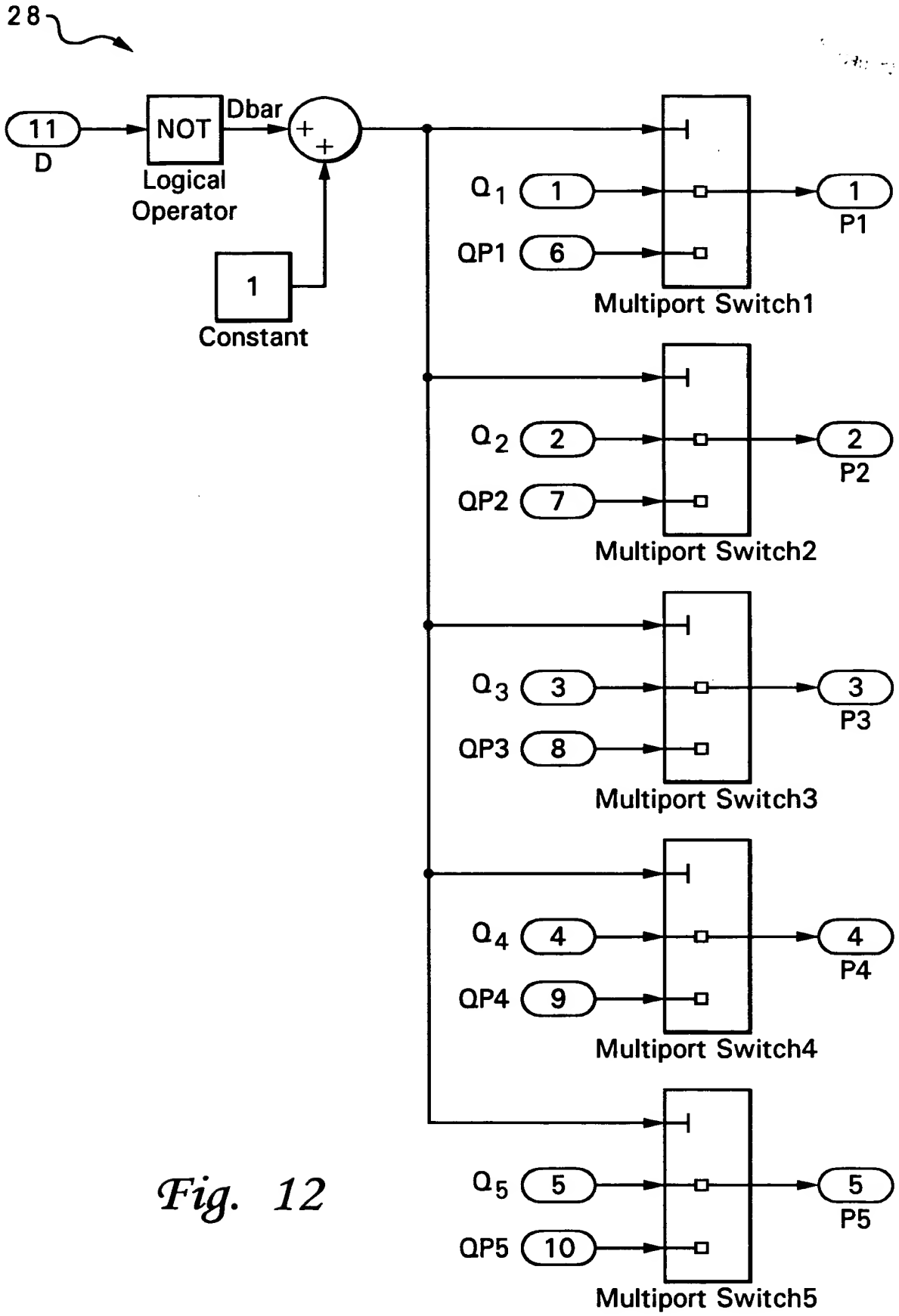
28
11
D
NOT
Logical
Operator
Dbar
+
+
1
Constant
Q1
1
QP1
6
1
P1
Multiport Switch1
Q2
2
QP2
7
2
P2
Multiport Switch2
Q3
3
QP3
8
3
P3
Multiport Switch3
Q4
4
QP4
9
4
P4
Multiport Switch4
Q5
5
QP5
10
5
P5
Multiport Switch5

Fig. 12

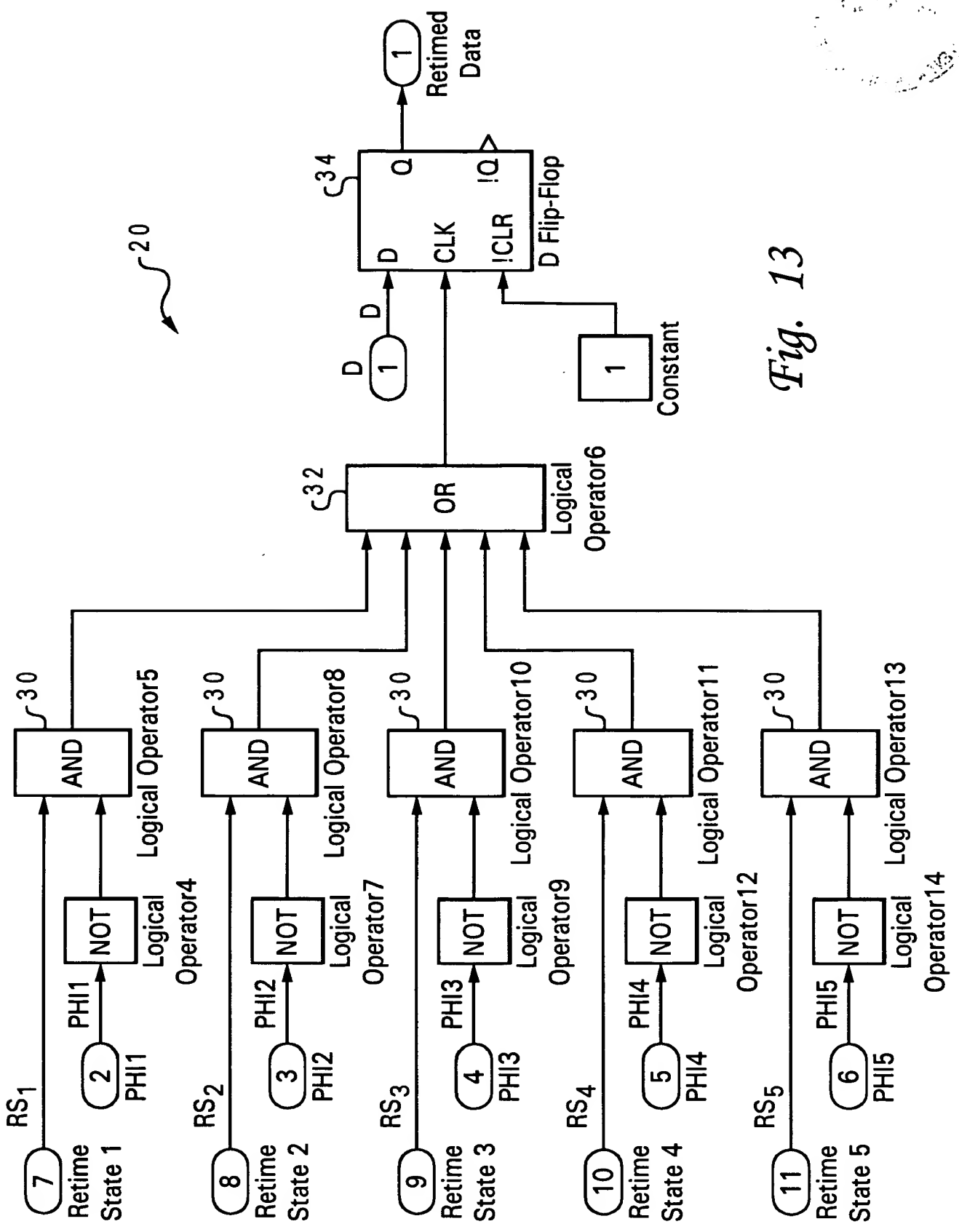
20
34
Retimed Data
1
Q
!Q
D
CLK
!CLR
D Flip-Flop
D
1
D
1
Constant
32
OR
Logical Operator6
30
AND
Logical Operator5
NOT
Logical Operator4
PHI1
2
PHI1
RS1
7
Retime State 1
Logical Operator8
Logical Operator7
PHI2
3
PHI2
RS2
8
Retime State 2
Logical Operator10
Logical Operator9
PHI3
4
PHI3
RS3
9
Retime State 3
Logical Operator11
Logical Operator12
PHI4
5
PHI4
RS4
10
Retime State 4
Logical Operator13
Logical Operator14
PHI5
6
PHI5
RS5
11
Retime State 5

Fig. 13

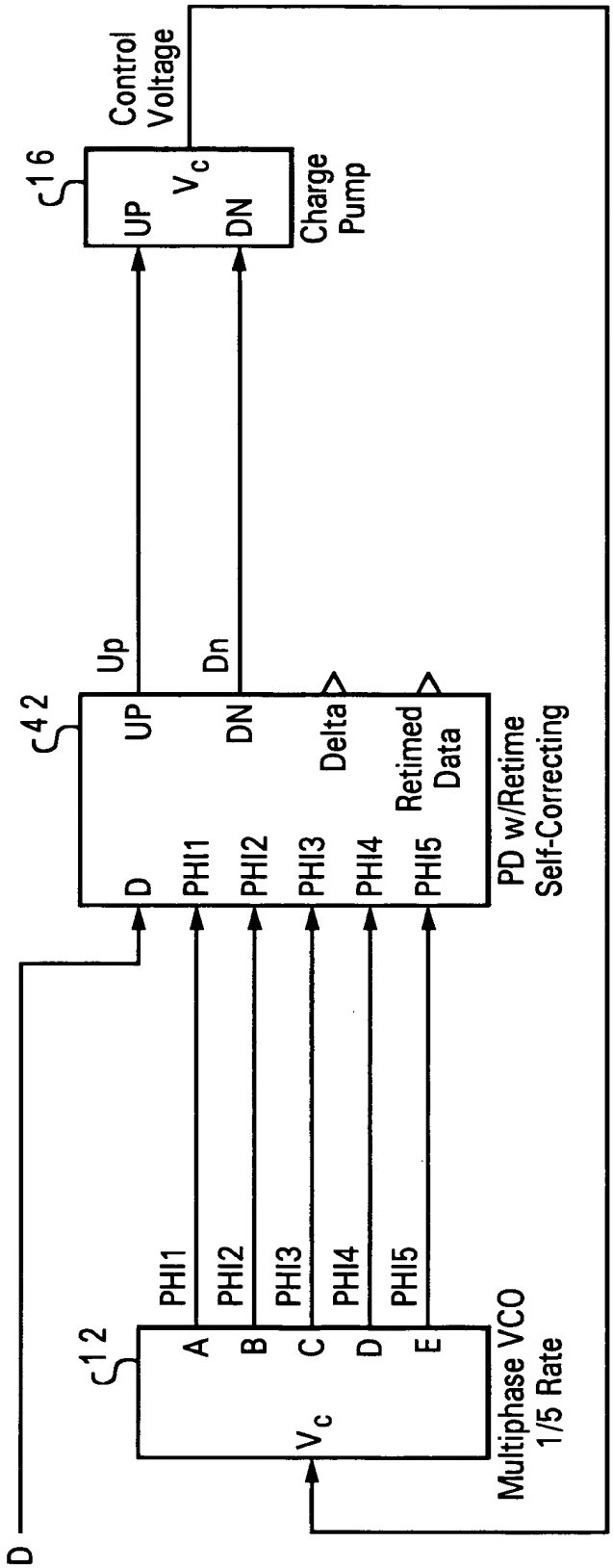
40
Control Voltage
16
UP
V_c
DN
Charge Pump
Up
Dn
42
UP
DN
Delta
Retimed Data
D
PHI1
PHI2
PHI3
PHI4
PHI5
PD w/Retime Self-Correcting
PHI1
PHI2
PHI3
PHI4
PHI5
12
A
B
C
D
E
V_c
Multiphase VCO 1/5 Rate
D

Fig. 14

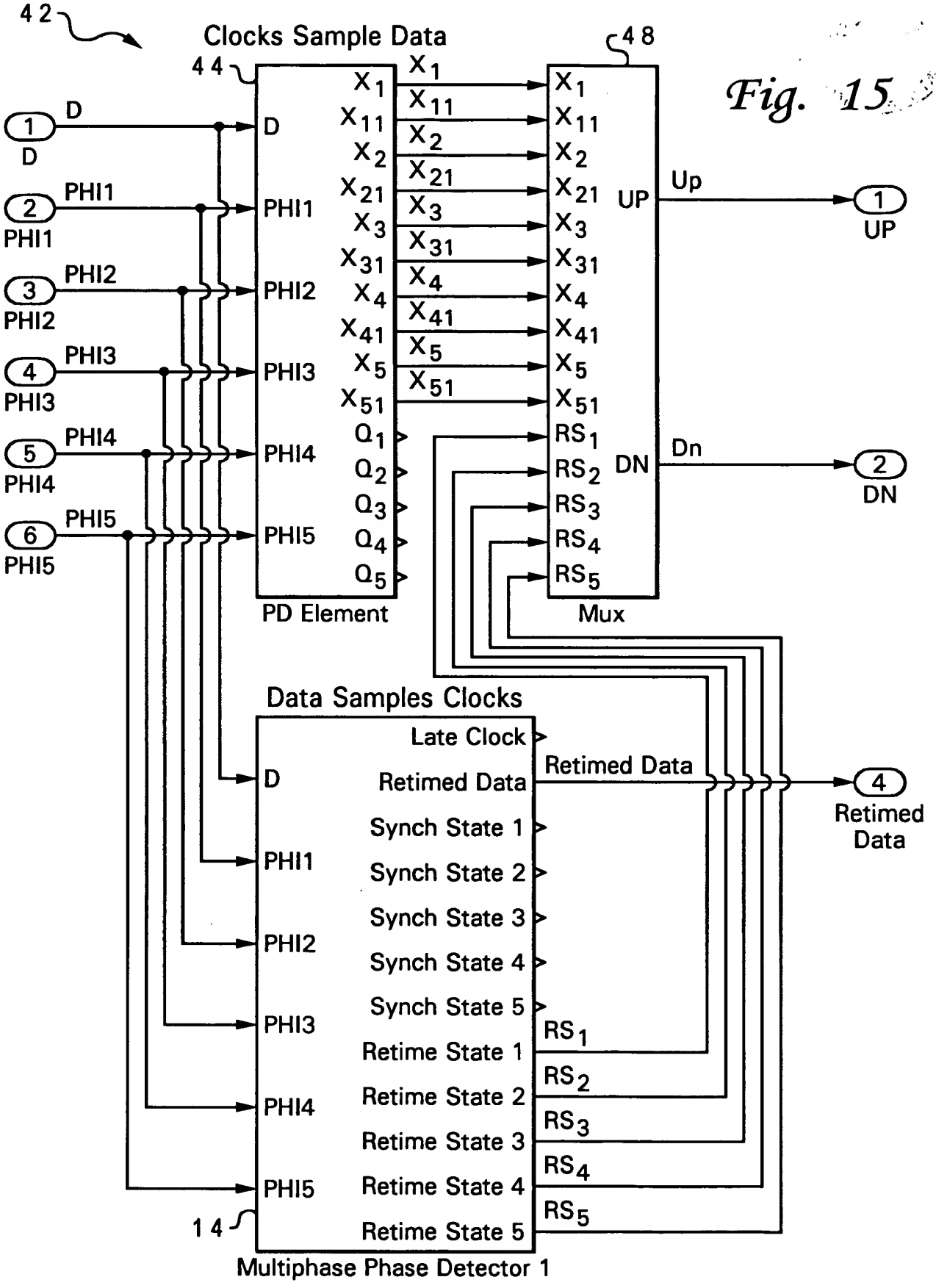
42
Clocks Sample Data
44
48
D
PHI1
PHI2
PHI3
PHI4
PHI5
PD Element
Mux
Up
UP
Dn
DN
Data Samples Clocks
Late Clock
Retimed Data
Synch State 1
Synch State 2
Synch State 3
Synch State 4
Synch State 5
Retime State 1
Retime State 2
Retime State 3
Retime State 4
Retime State 5
14
Multiphase Phase Detector 1

Fig. 15

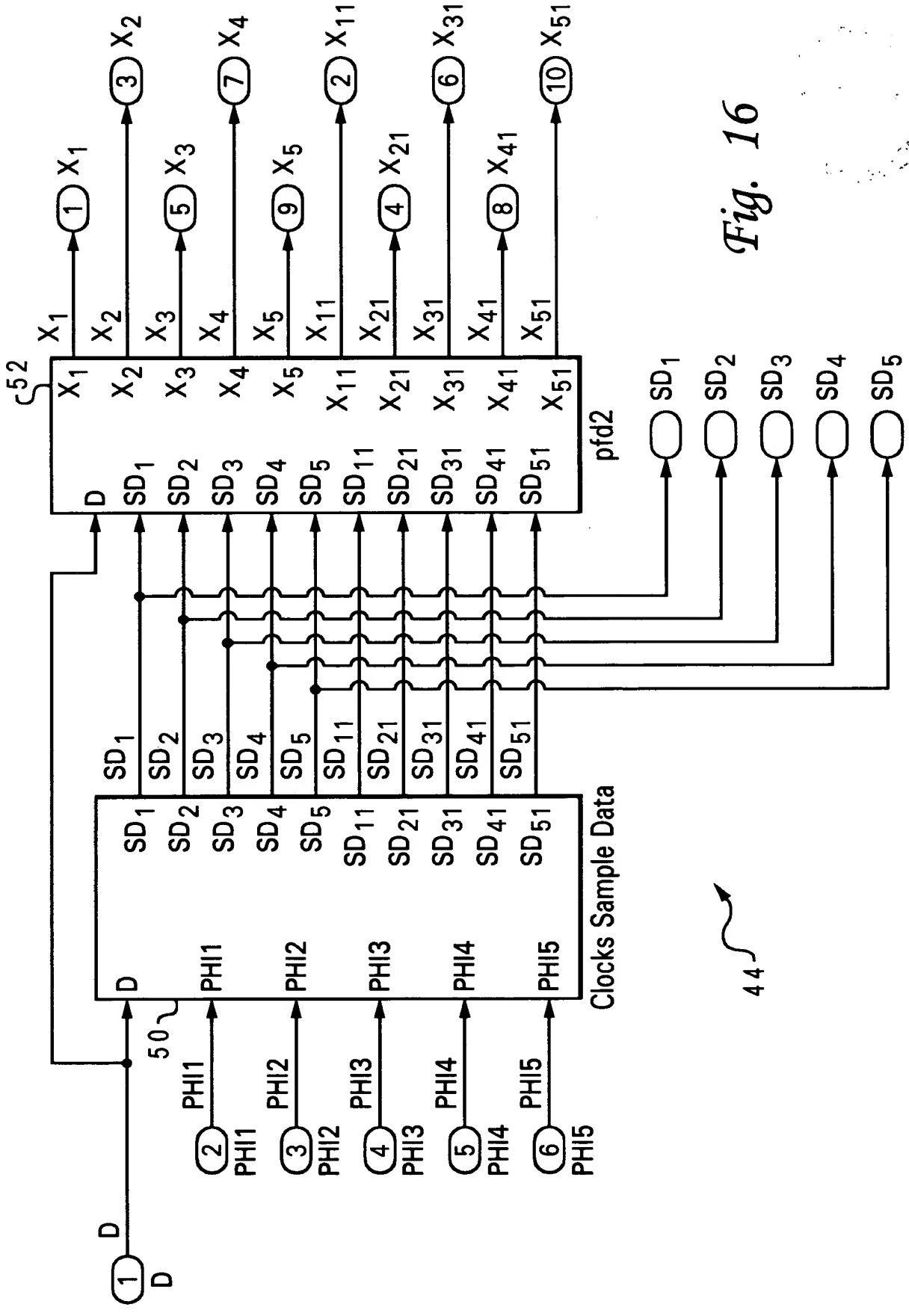
X1
X2
X3
X4
X5
X11
X21
X31
X41
X51
pfd2
D
SD1
SD2
SD3
SD4
SD5
SD11
SD21
SD31
SD41
SD51
Clocks Sample Data
PHI1
PHI2
PHI3
PHI4
PHI5
50
52
44

Fig. 16

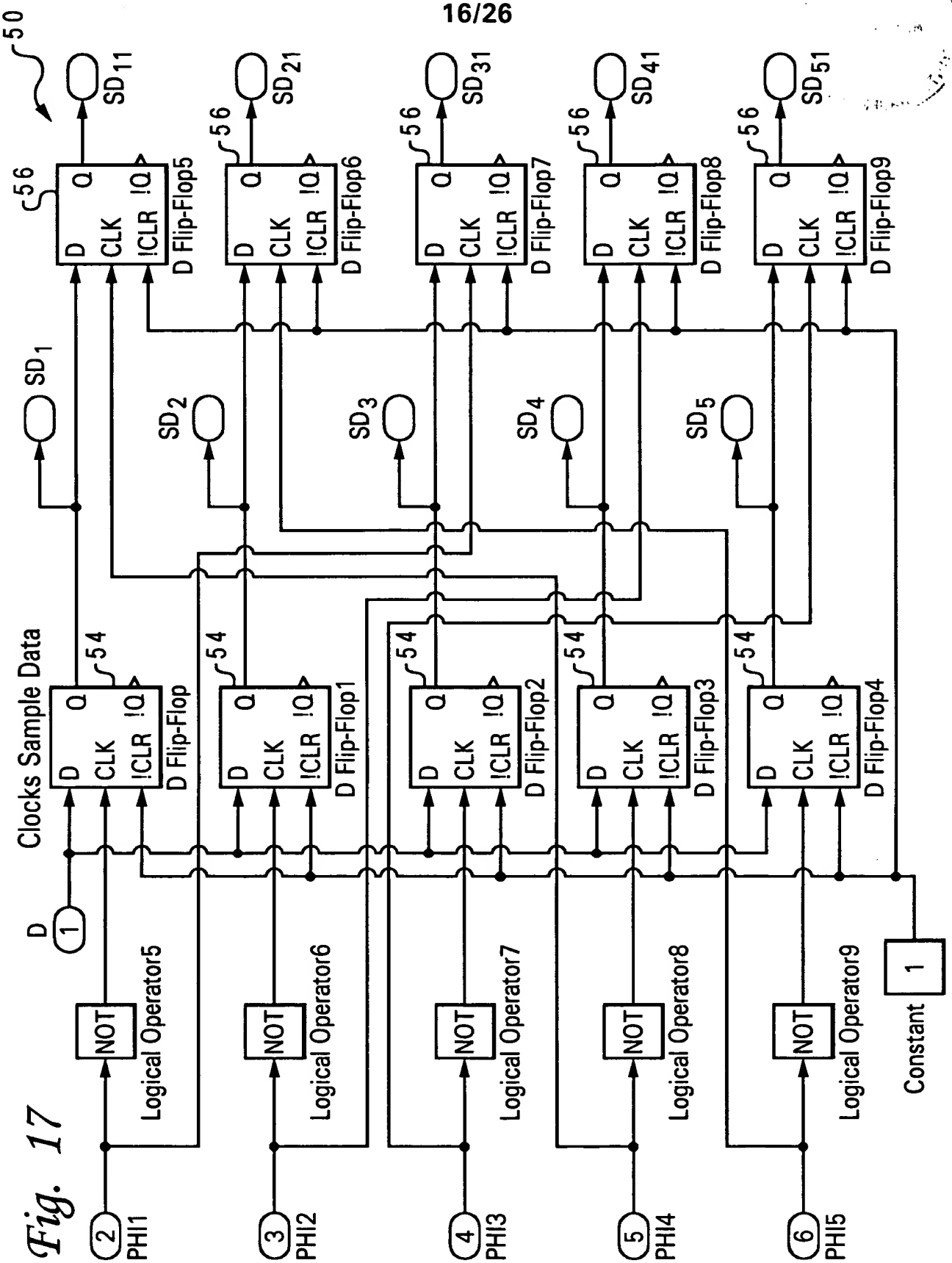
50
SD11
SD21
SD31
SD41
SD51
56
D Flip-Flop5
D Flip-Flop6
D Flip-Flop7
D Flip-Flop8
D Flip-Flop9
SD1
SD2
SD3
SD4
SD5
Clocks Sample Data
54
D Flip-Flop
D Flip-Flop1
D Flip-Flop2
D Flip-Flop3
D Flip-Flop4
D
1
NOT
Logical Operator5
Logical Operator6
Logical Operator7
Logical Operator8
Logical Operator9
Constant
2
PHI1
3
PHI2
4
PHI3
5
PHI4
6
PHI5

Fig. 17

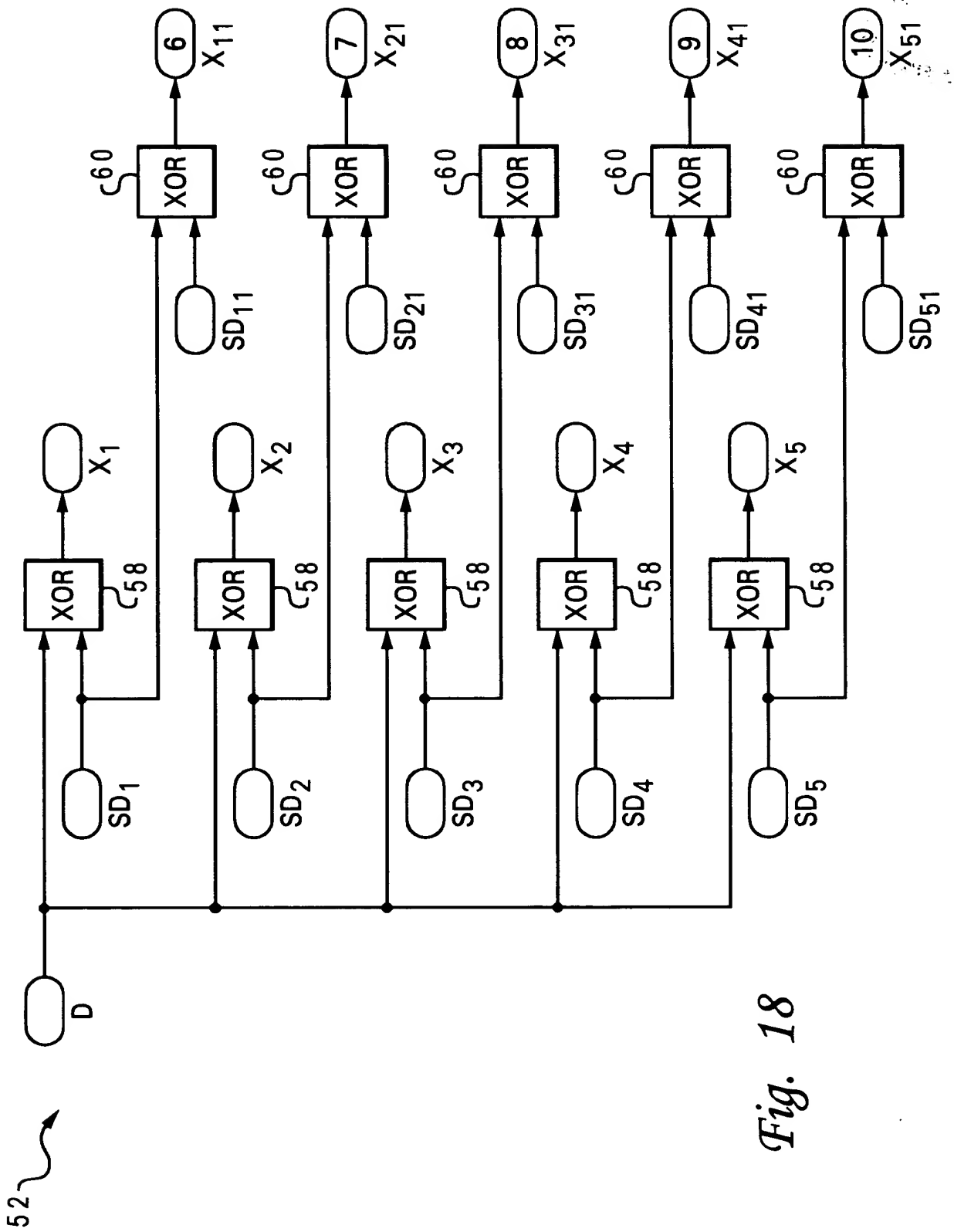
52
D
X1
X2
X3
X4
X5
SD1
SD2
SD3
SD4
SD5
XOR
58
60
6
7
8
9
10
X11
X21
X31
X41
X51
SD11
SD21
SD31
SD41
SD51

Fig. 18

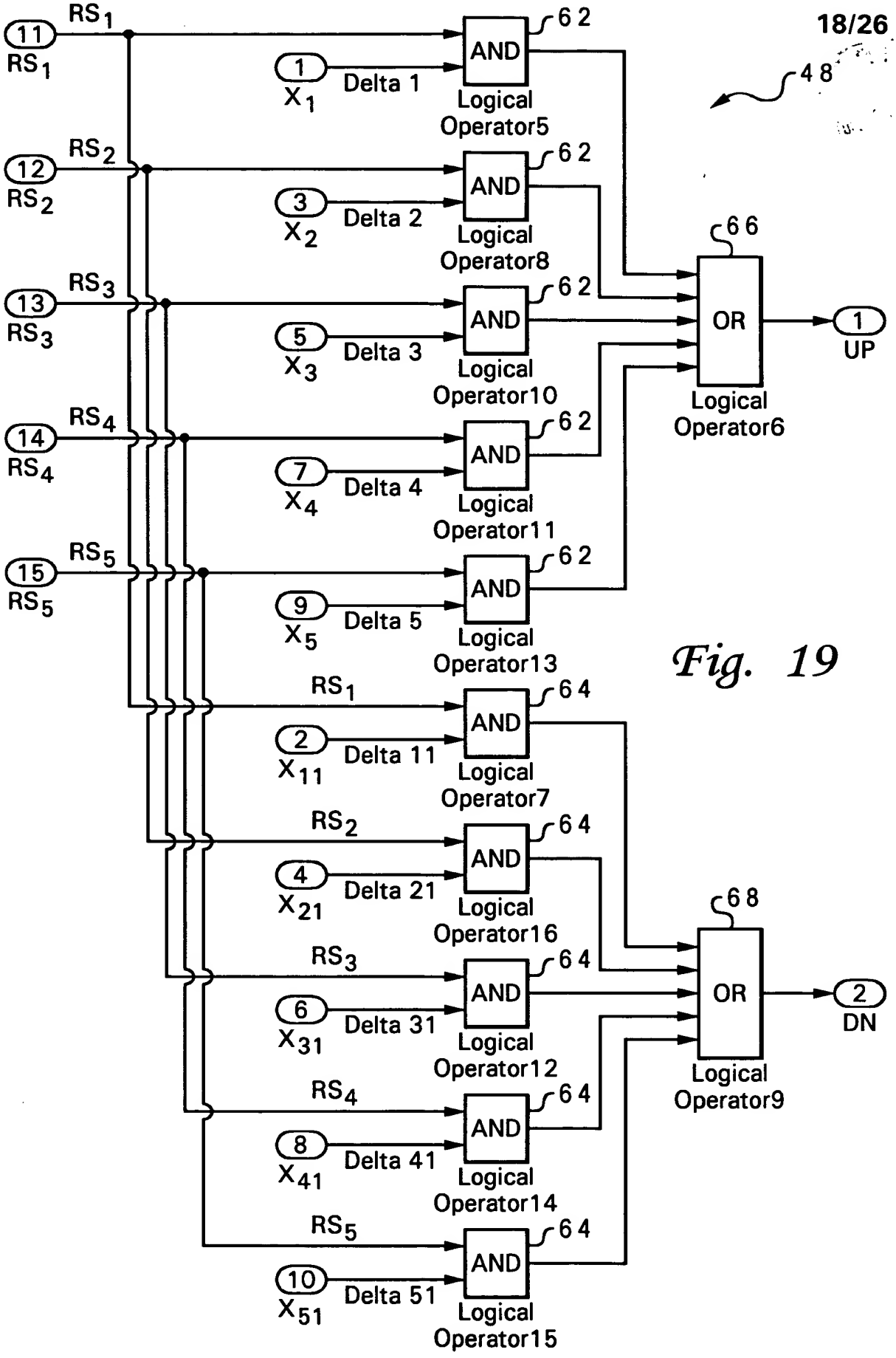
48
11
RS1
RS1
1
X1
Delta 1
AND
62
Logical
Operator5
12
RS2
RS2
3
X2
Delta 2
AND
62
Logical
Operator8
13
RS3
RS3
5
X3
Delta 3
AND
62
Logical
Operator10
14
RS4
RS4
7
X4
Delta 4
AND
62
Logical
Operator11
15
RS5
RS5
9
X5
Delta 5
AND
62
Logical
Operator13
66
OR
1
UP
Logical
Operator6
RS1
2
X11
Delta 11
AND
64
Logical
Operator7
RS2
4
X21
Delta 21
AND
64
Logical
Operator16
RS3
6
X31
Delta 31
AND
64
Logical
Operator12
RS4
8
X41
Delta 41
AND
64
Logical
Operator14
RS5
10
X51
Delta 51
AND
64
Logical
Operator15
68
OR
2
DN
Logical
Operator9

Fig. 19

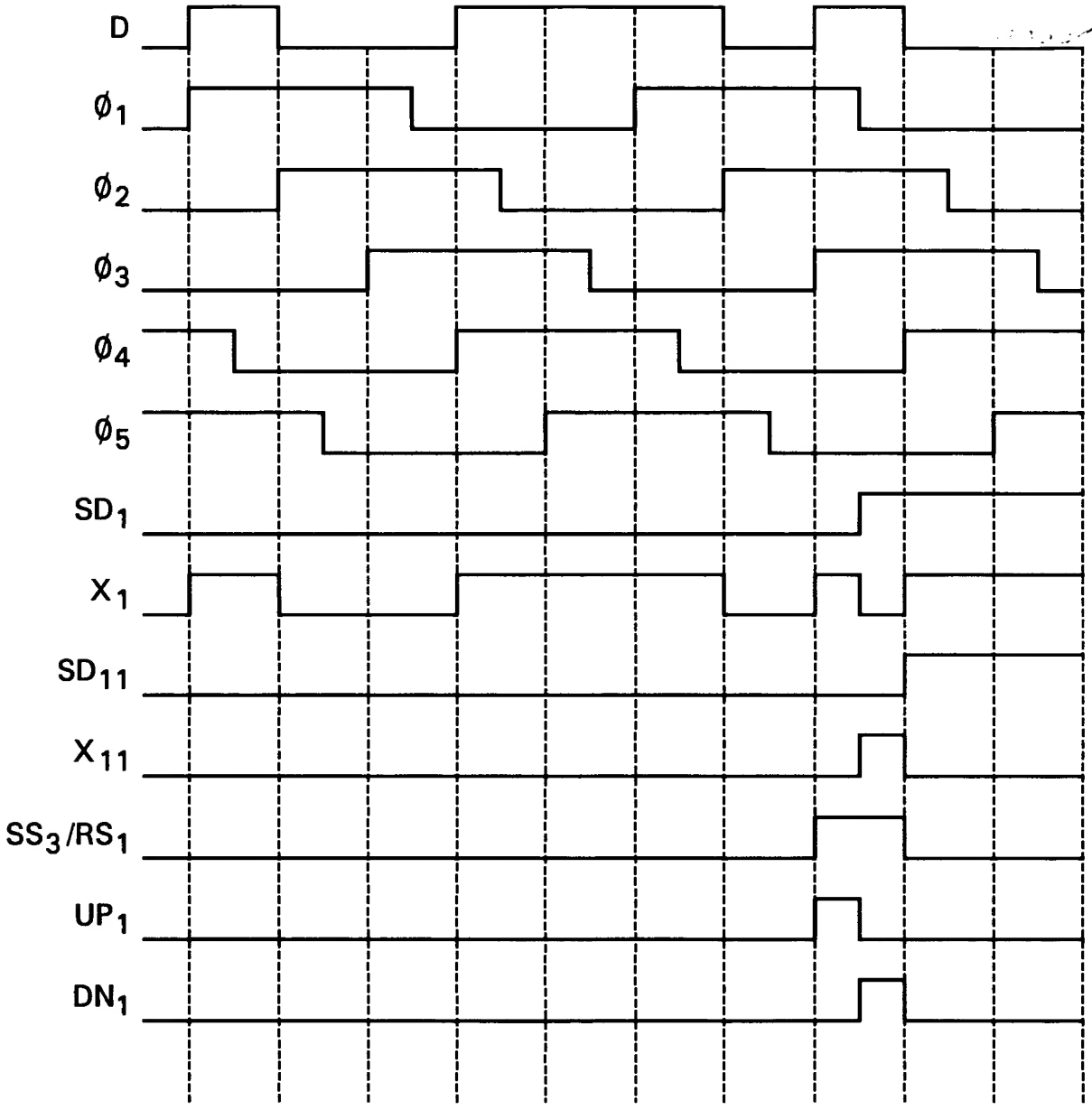

Fig. 20

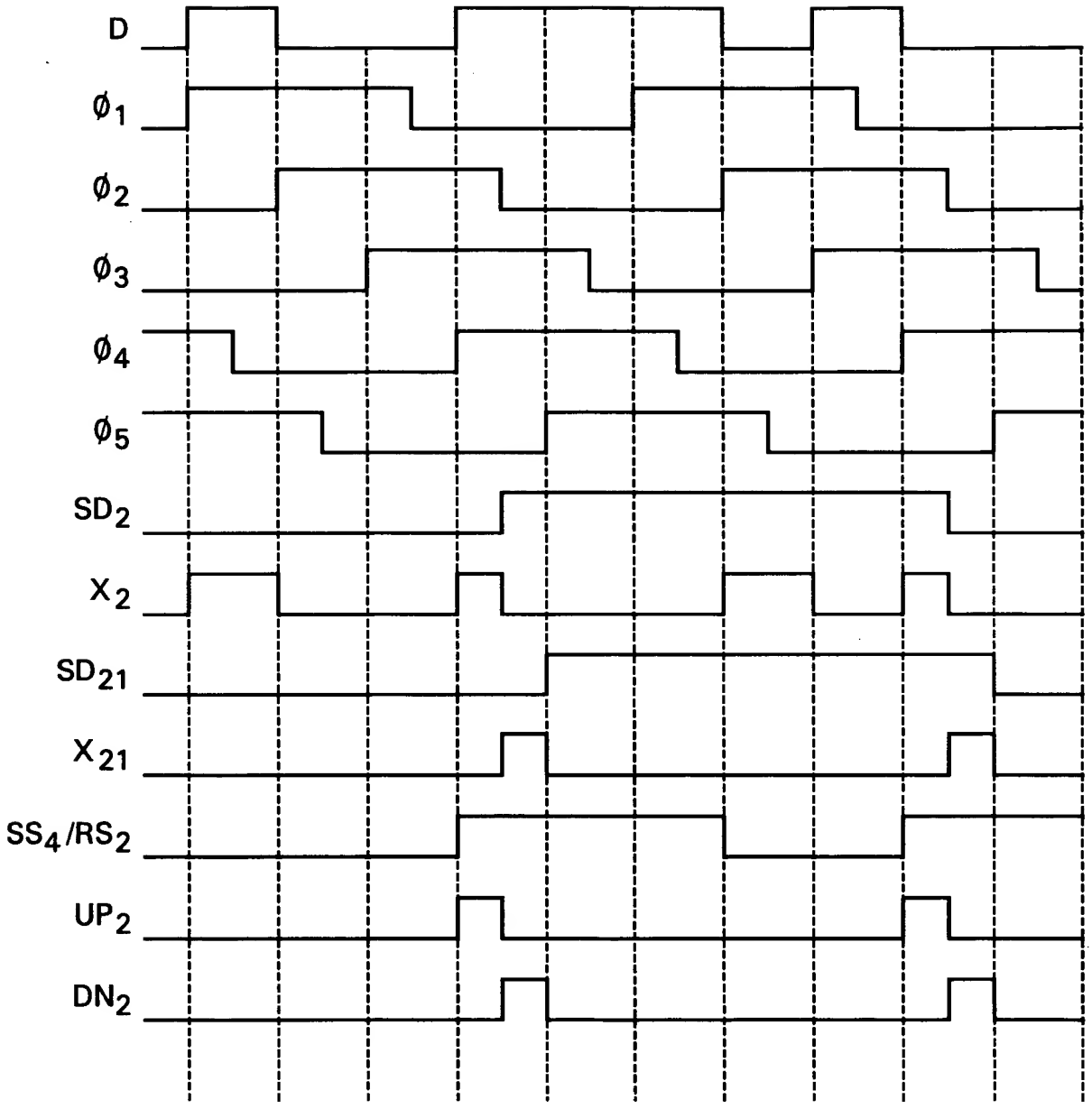

Fig. 21

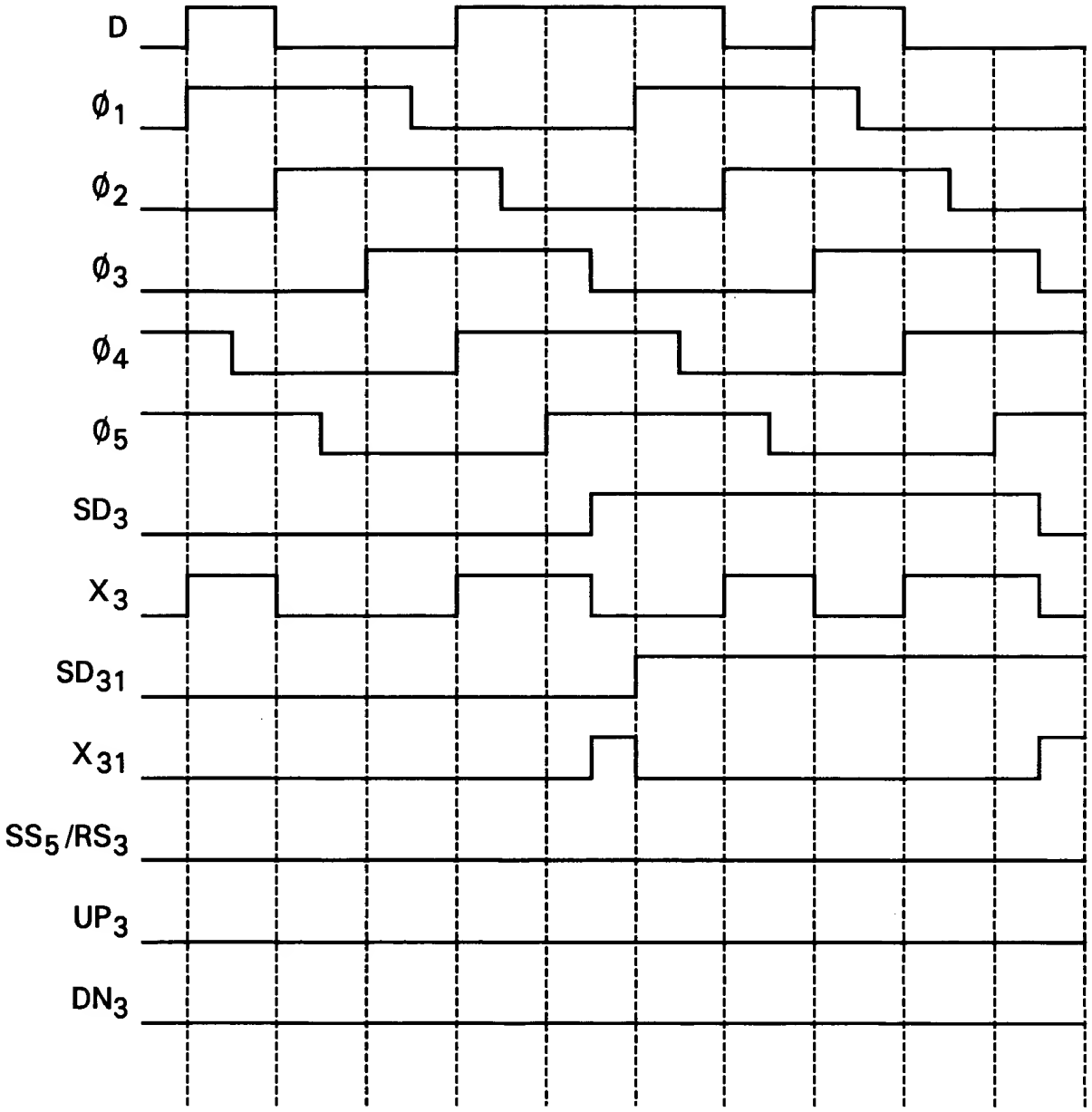

Fig. 22

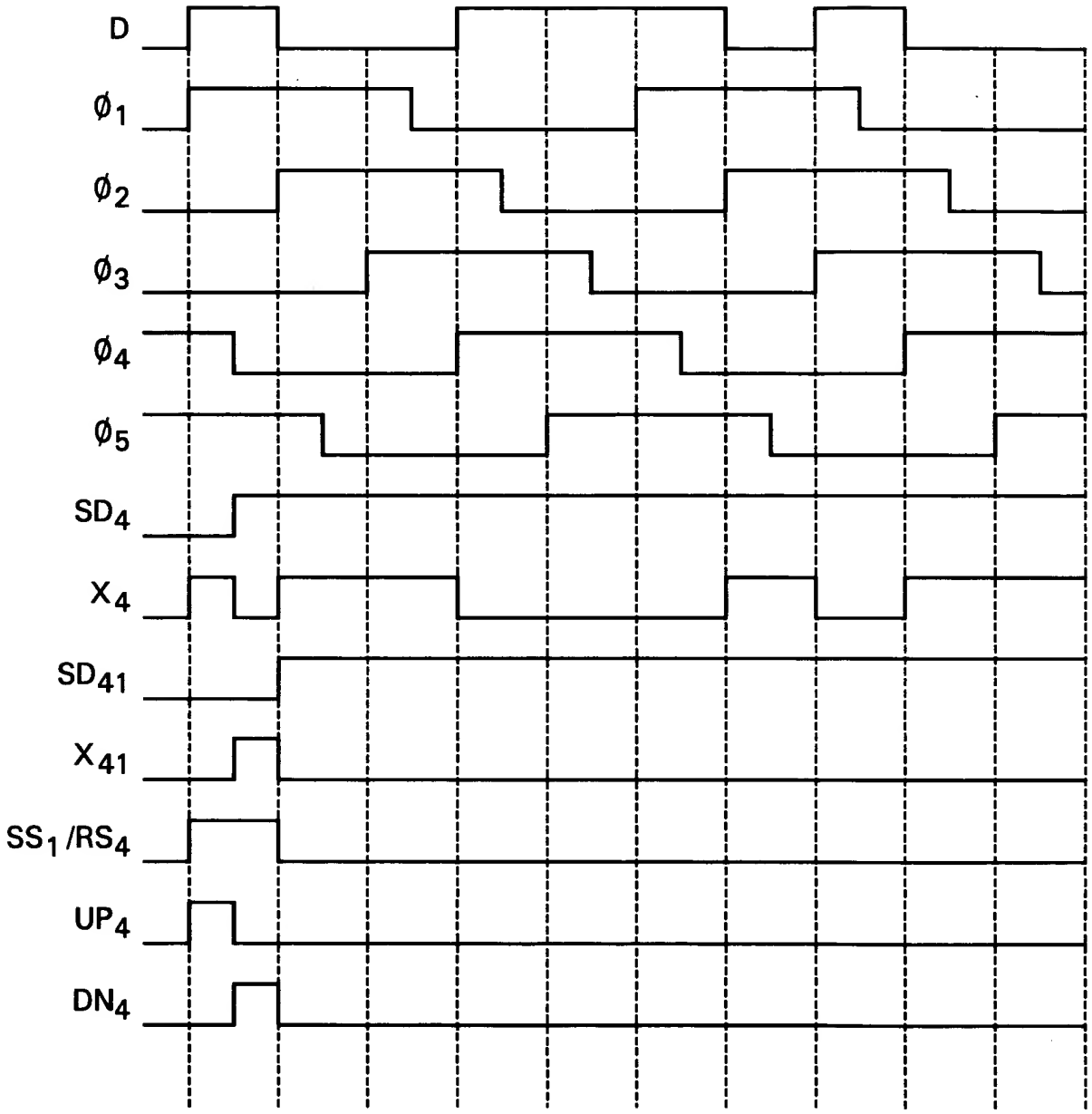

Fig. 23

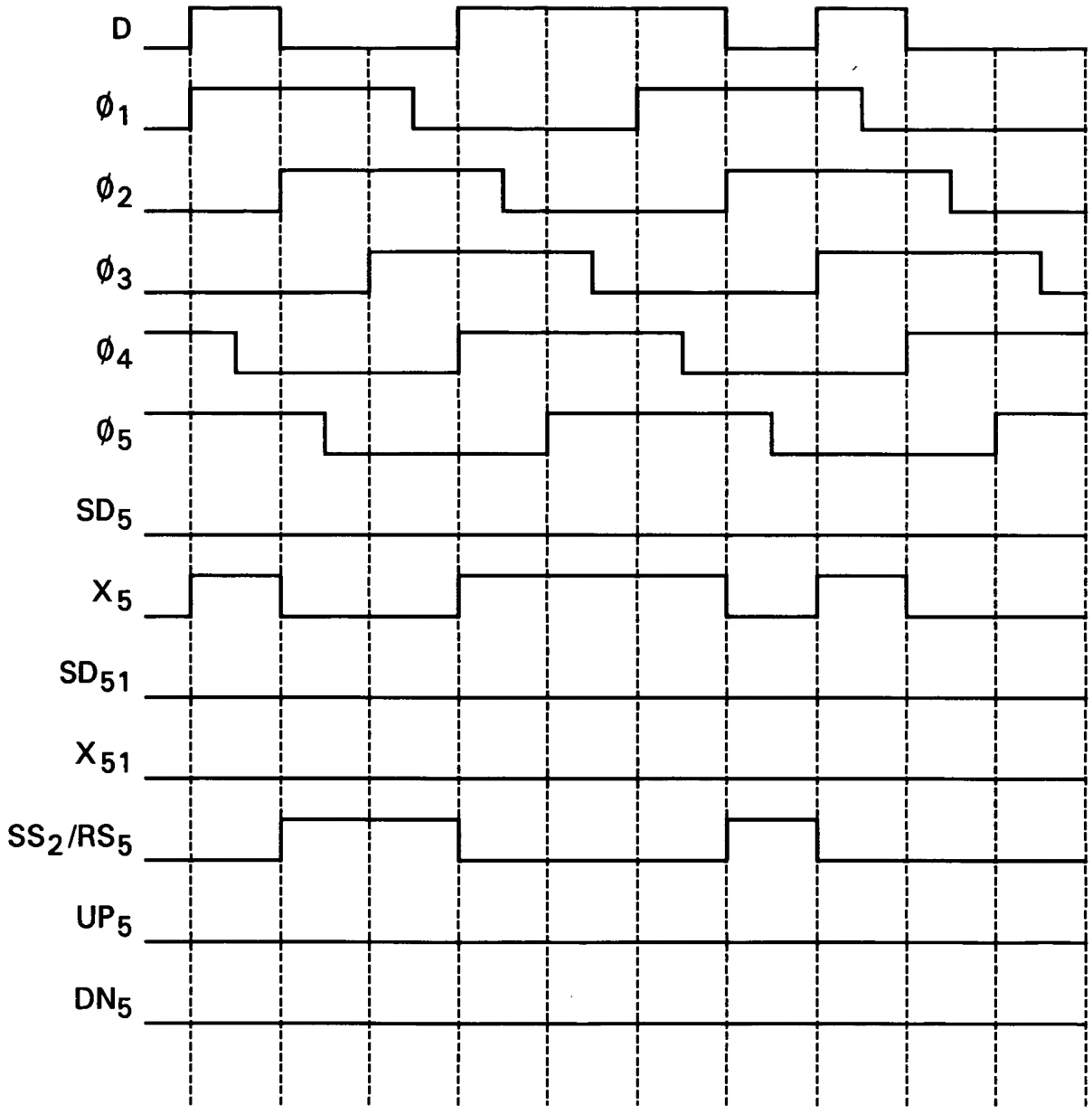

Fig. 24

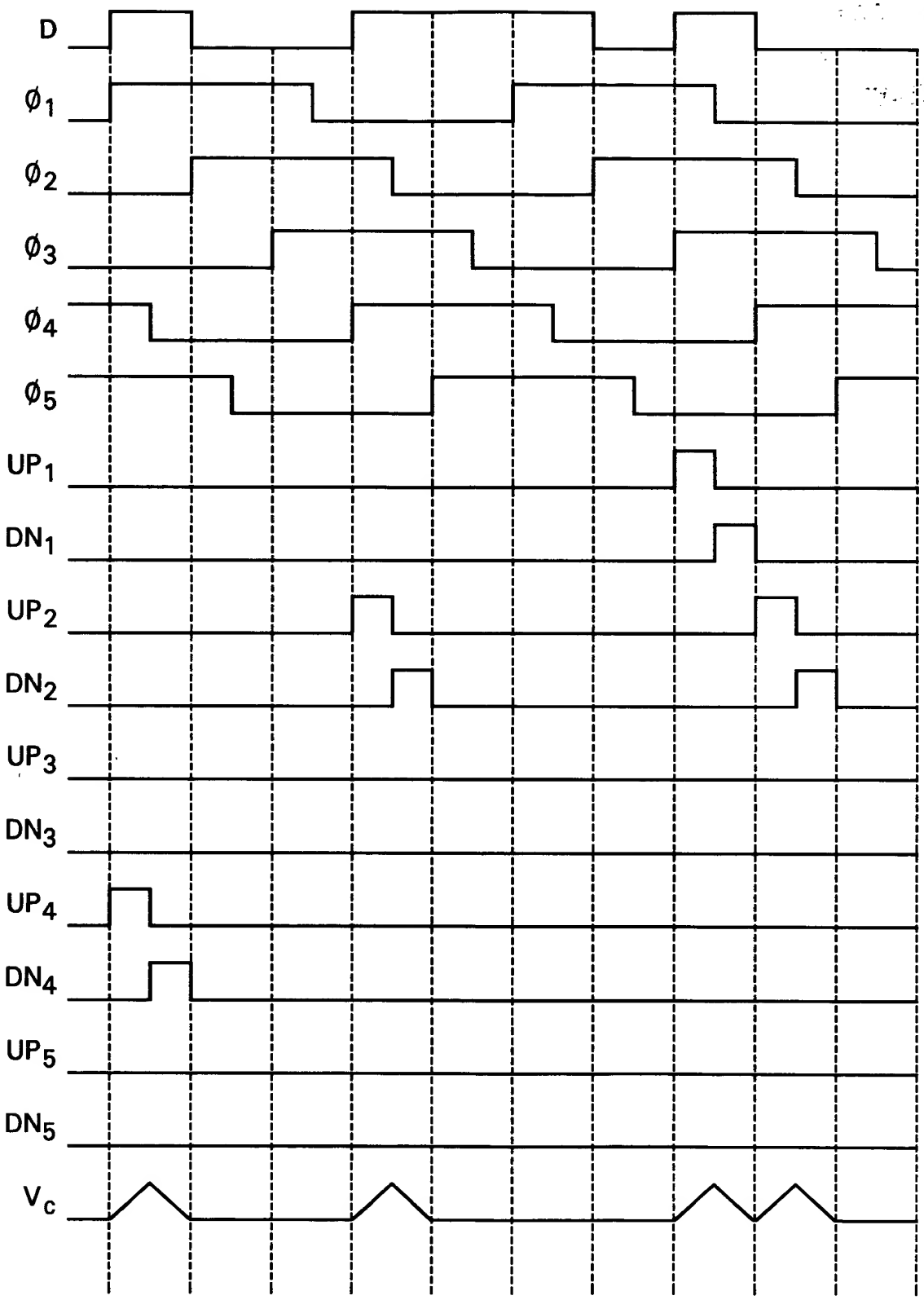
D
ϕ_1
ϕ_2
ϕ_3
ϕ_4
ϕ_5
UP_1
DN_1
UP_2
DN_2
UP_3
DN_3
UP_4
DN_4
UP_5
DN_5
V_c

Fig. 25

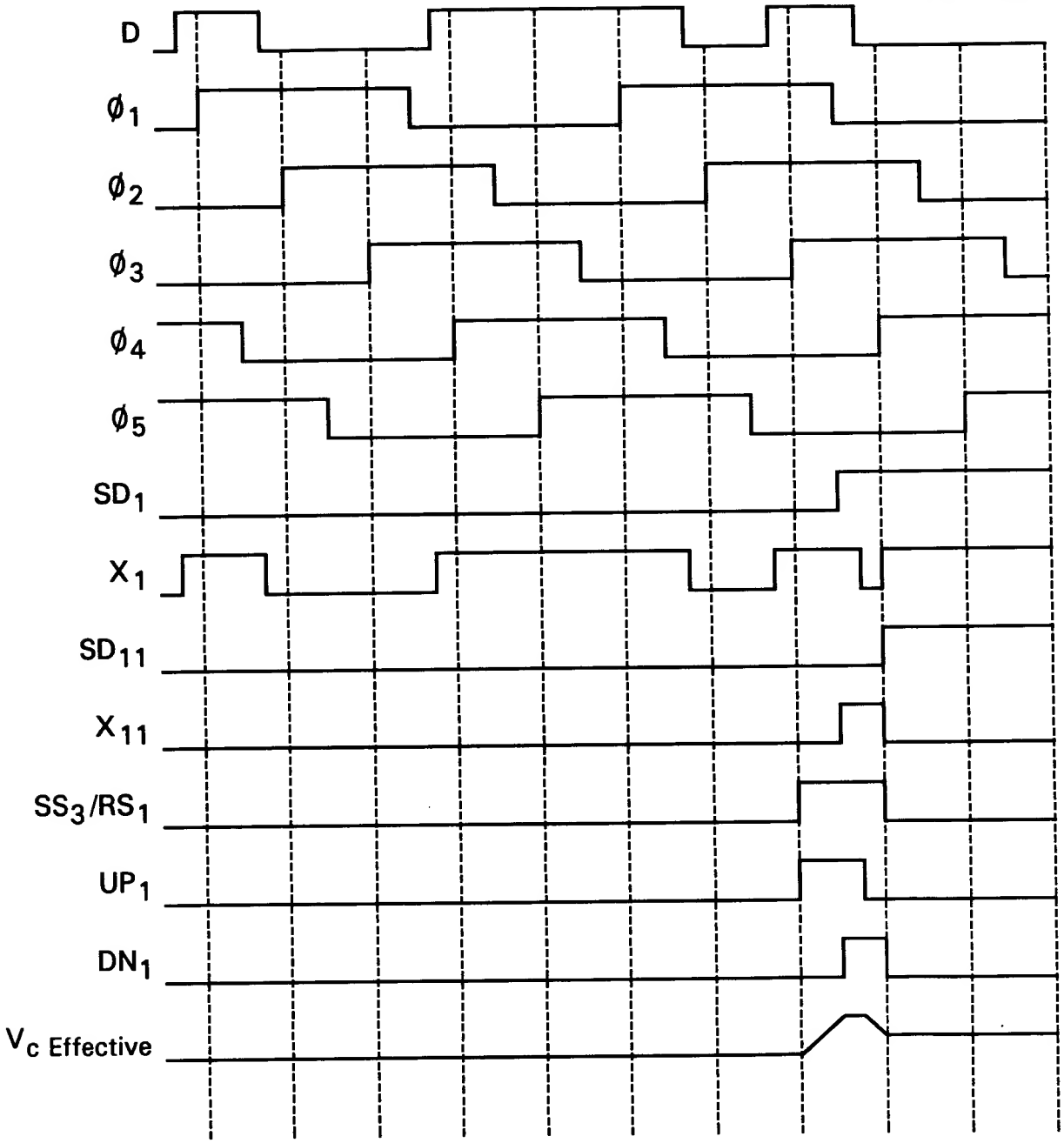
D
ϕ_1
ϕ_2
ϕ_3
ϕ_4
ϕ_5
SD_1
X_1
SD_{11}
X_{11}
SS_3/RS_1
UP_1
DN_1
V_c Effective

Fig. 26

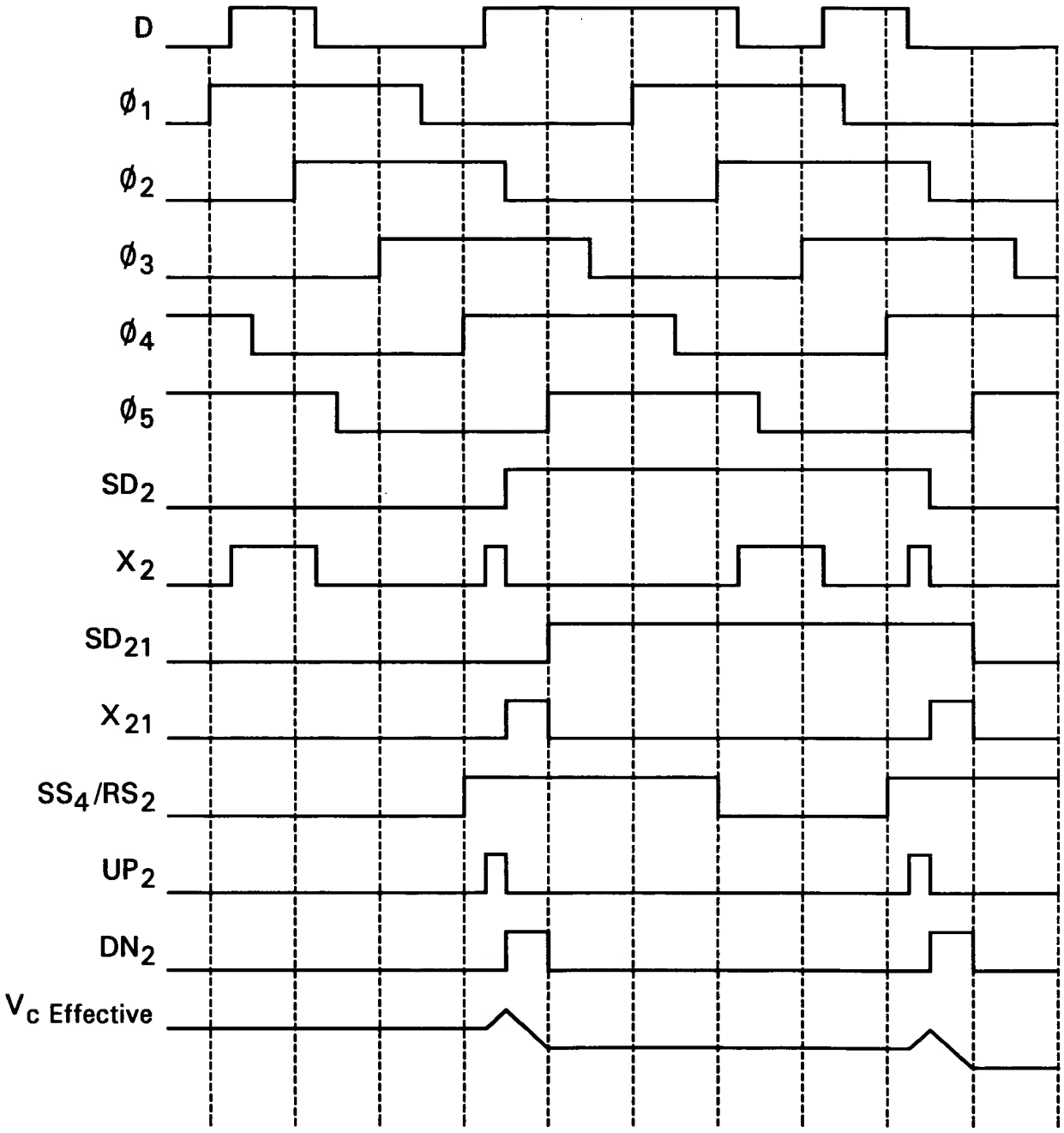
D
ϕ_1
ϕ_2
ϕ_3
ϕ_4
ϕ_5
SD_2
X_2
SD_{21}
X_{21}
SS_4/RS_2
UP_2
DN_2
V_c Effective

Fig. 27